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## PATENT APPLICATION FULL TEXT AND IMAGE DATABASE



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Multistandard video decoder and decompression system for processing encoded bit streams including pipeline processing and methods relating thereto

### Abstract

A pipeline video decoder and decompression system handles a plurality of separately encoded bit streams arranged as a single serial bit stream of digital bits and having separately encoded pairs of control codes and corresponding data carried in the serial bit stream. The pipeline system employs a plurality of interconnected stages to decode and decompress the single bit stream, including a start code detector. When in a search mode, the start code detector searches for a specific start code corresponding to one of multiple compression standards. The start code detector responding to the single serial bit stream generates control tokens and data tokens. A respective one of the tokens includes a plurality of data words. Each data word has an extension bit which indicates a presence of additional words therein. The data words are thereby unlimited in number. A token decode circuit positioned in certain of the stages recognizes certain of the tokens as control tokens pertinent to that stage and passes unrecognized control tokens to a succeeding stage. A reconfigurable decode and parser processing means positioned in certain of the stages is responsive to a recognized control token and reconfigures a particular stage to handle an identified data token. Methods relating to the decoder and decompression system include processing steps relating thereto

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### Claims

1. A pipeline system for decoding a data stream of data having portions encoded according to different standards comprising: a sequence of pipeline stages, at least one of the pipeline stages being reconfigurable to operate according to the different standards; the at least one of the pipeline stages including processing circuitry with an active state which is entered when the data received by the at least one of the pipeline stages has a predetermined activation pattern, the predetermined activation pattern corresponding to one of the different standards; the at least one of the pipeline stages including a state machine having a current state and a previous state; and wherein the at least one of the pipeline stages is activated upon recognition of the predetermined activation pattern only upon a predetermined transition from the previous state to the current state.
2. The pipeline system of claim 1, wherein the processing circuitry has an inactive state, in which the at least one of the pipeline stages passes data to a following pipeline stage without processing.
3. The pipeline system of claim 1, wherein the sequence of pipeline stages includes at least one spatial decoder stage.
4. The pipeline system of claim 1, wherein the sequence of pipeline stages includes at least one temporal decoder stage.
5. The pipeline system of claim 1, wherein the at least one of the pipeline stages is a spatial decoder stage.
6. The pipeline system of claim 1, wherein the at least one of the pipeline stages is a temporal decoder stage.

### Description

[0001] This is a continuation-in-part application of U.S. Serial No. (not yet known) filed Feb. 2, 1995, which is a continuation application of Serial No. 08/082,291 filed Jun. 24, 1993. This application claims priority from EPO Application No. 92306038.8 filed June 30, 1992, British Application No. 9405914.4 filed Mar. 24, 1994 and British Application No. (not yet known) filed Feb. 28, 1995.

#### BACKGROUND OF THE INVENTION

[0002] The present invention is directed to improvements in methods and apparatus for decompression which operates to decompress and/or decode a plurality of differently encoded input signals. The illustrative embodiment chosen for description hereinafter relates to the decoding of a plurality of encoded picture standards. More specifically, this embodiment relates to the decoding of any one of the well known standards known as JPEG, MPEG and H.201.

[0003] A serial pipeline processing system of the present invention comprises a single two-wire bus used for carrying unique and specialized interactive interfacing tokens, in the form of control tokens and data tokens, to a plurality of adaptive decompression circuits and the like positioned as a reconfigurable pipeline processor.

[0004] Video compression/decompression systems are generally well-known in the art. However, such systems have generally been dedicated in design and use to a single compression standard. They have also suffered from a number of other inefficiencies and inflexibility in overall system and